# Four Degrees of Freedom Inertial Sensor

# ADIS16300

## FEATURES

**14-bit digital gyroscope with digital range scaling**
**±75°/sec, ±150°/sec, ±300°/sec settings**
**Tri-axis, 14-bit digital accelerometer**
**±3 *g* measurement range**
**13-bit pitch and roll incline calculations**
**330 Hz bandwidth**
**150 ms start-up time**
**Factory-calibrated sensitivity, bias, and axial alignment**
**Digitally controlled bias calibration**
**Digitally controlled sample rate, up to 819.2 SPS**
**External clock input enables sample rates up to 1200 SPS**
**Digitally controlled filtering**
**Programmable condition monitoring**
**Auxiliary digital input/output**
**Digitally activated self-test**
**Programmable power management**
**Embedded temperature sensor**
**SPI-compatible serial interface**
**Auxiliary, 12-bit ADC input and DAC output**
**Single-supply operation: 4.75 V to 5.25 V**
**2000 *g* shock survivability**
**Operating temperature range: −40°C to +85°C**

## APPLICATIONS

**Medical instrumentation**
**Robotics**
**Platform control**
**Navigation**

## FUNCTIONAL BLOCK DIAGRAM

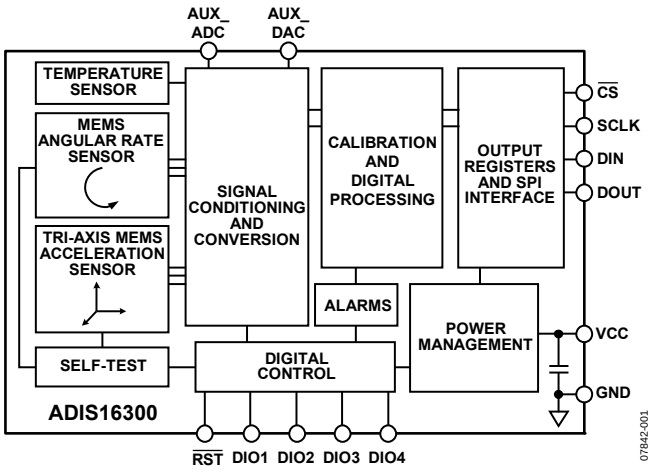



*Figure 1.*

## GENERAL DESCRIPTION

The ADIS16300 *i*Sensor® is a complete inertial system that includes a yaw rate gyroscope and tri-axis accelerometer. Each sensor in the ADIS16300 combines industry-leading *i*MEMS® technology with signal conditioning that optimizes dynamic performance. The factory calibration characterizes each sensor for sensitivity, bias, alignment, and linear acceleration (gyro bias). As a result, each sensor has its own dynamic compensation for correction formulas that provide accurate sensor measurements over the specified power supply range of +4.75 V to +5.25 V. The ADIS16300 provides a simple, cost-effective method for integrating accurate, multi-axis, inertial sensing into industrial systems, especially when compared with the complexity and investment associated with discrete designs. All necessary motion testing and calibration are part of the production process at the factory, greatly reducing system integration time. Tight orthogonal alignment simplifies inertial frame alignment in navigation systems. An improved SPI interface and register structure provide faster data collection and configuration control. The ADIS16300, along with a flex interface, drops into current systems that use the ADIS1635x family, providing the opportunity to scale cost for systems that only require four degrees of freedom inertial sensing. This compact module is approximately 23 mm × 31 mm × 7.5 mm and provides a standard connector interface, which enables horizontal or vertical mounting.

**Rev. A**


**One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.**
**Tel: 781.329.4700** **www.analog.com**
**Fax: 781.461.3113** 

# TABLE OF CONTENTS

Features ..... 1
Applications ..... 1
Functional Block Diagram ..... 1
General Description ..... 1
Revision History ..... 2
Specifications ..... 3
Timing Specifications ..... 5
Timing Diagrams ..... 5
Absolute Maximum Ratings ..... 6
ESD Caution ..... 6
Pin Configuration and Function Descriptions ..... 7
Typical Performance Characteristics ..... 8
Basic Operation ..... 9
Reading Sensor Data ..... 9
Device Configuration ..... 9
Burst Mode Data Collection ..... 9
Output Data Registers ..... 11
Calibration ..... 11
Operational Control ..... 12
Input/Output Functions ..... 13
Diagnostics ..... 14
Outline Dimensions ..... 16
Ordering Guide ..... 16

## REVISION HISTORY

**4/09—Rev. 0 to Rev. A**

Changes to Figure 5 and Figure 6 ..... 7
Changes to Figure 7 ..... 8
Changes to Ordering Guide ..... 16

**10/08—Revision 0: Initial Version**

# SPECIFICATIONS

$T_A$ = −40°C to +85°C, VCC = 5.0 V, angular rate = 0°/sec, dynamic range = ±300°/sec, ±1 *g*, unless otherwise noted.

**Table 1.**

| Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| GYROSCOPE | | | | | |
| Dynamic Range | | ±300 | ±375 | | °/sec |
| Initial Sensitivity | $T_A$ = 25°C, dynamic range = ±300°/sec | 0.0495 | 0.05 | 0.0505 | °/sec/LSB |
| | $T_A$ = 25°C, dynamic range = ±150°/sec | | 0.025 | | °/sec/LSB |
| | $T_A$ = 25°C, dynamic range = ±75°/sec | | 0.0125 | | °/sec/LSB |
| Sensitivity Temperature Coefficient | | | 400 | | ppm/°C |
| Misalignment | Reference to z-axis accelerometer, $T_A$ = 25°C | | 0.1 | | Degrees |
| | Axis-to-frame (package), $T_A$ = 25°C | | ±0.5 | | Degrees |
| Nonlinearity | Best fit straight line | | 0.1 | | % of FS |
| Initial Bias Error | $T_A$ = 25°C, ±1 σ | | ±3 | | °/sec |
| In-Run Bias Stability | $T_A$ = 25°C, 1 σ, SMPL_PRD = 0x01 | | 0.007 | | °/sec |
| Angular Random Walk | $T_A$ = 25°C, 1 σ, SMPL_PRD = 0x01 | | 1.9 | | °/√hr |
| Bias Temperature Coefficient | | | 0.1 | | °/sec/°C |
| Linear Acceleration Effect on Bias | Any axis, 1 σ (MSC_CTRL Bit [7] = 1) | | 0.05 | | °/sec/*g* |
| Voltage Sensitivity | VCC = 4.75 V to 5.25 V | | 0.25 | | °/sec/V |
| Output Noise | $T_A$ = 25°C, ±300°/sec range, no filtering | | 1.1 | | °/sec rms |
| Rate Noise Density | $T_A$ = 25°C, f = 25 Hz, ±300°/sec, no filtering | | 0.038 | | °/sec/√Hz rms |
| 3 dB Bandwidth | | | 330 | | Hz |
| Sensor Resonant Frequency | | | 14.5 | | kHz |
| Self-Test Change in Output Response | ±300°/sec range setting | ±696 | ±1400 | ±2449 | LSB |
| ACCELEROMETERS | Each axis | | | | |
| Dynamic Range | | ±3 | ±3.6 | | *g* |
| Initial Sensitivity | 25°C | 0.594 | 0.6 | 0.606 | m*g*/LSB |
| Sensitivity Temperature Coefficient | X axis and Y axis | | 250 | | ppm/°C |
| | Z axis | | 300 | | ppm/°C |
| Misalignment | Axis-to-axis, $T_A$ = 25°C, Δ = 90° ideal | | ±0.25 | | Degrees |
| | Axis-to-frame (package), $T_A$ = 25°C | | ±0.5 | | Degrees |
| Nonlinearity | Best fit straight line | | ±0.3 | | % of FS |
| Initial Bias Error | $T_A$ = 25°C, ±1 σ, X axis and Y axis | | ±60 | | m*g* |
| | $T_A$ = 25°C, ±1 σ, Z axis | | ±110 | | m*g* |
| In-Run Bias Stability | $T_A$ = 25°C, 1 σ, X axis and Y axis | | 0.048 | | m*g* |
| | $T_A$ = 25°C, 1 σ, Z axis | | 0.054 | | m*g* |
| Velocity Random Walk | $T_A$ = 25°C, 1 σ, X axis and Y axis | | 0.118 | | m/sec/√hr |
| | $T_A$ = 25°C, 1 σ, Z axis | | 0.164 | | m/sec/√hr |
| Bias Temperature Coefficient | X axis and Y axis | | 2.5 | | m*g*/°C |
| | Z axis | | 4.5 | | m*g*/°C |
| Output Noise | $T_A$ = 25°C, no filtering, X axis and Y axis | | 5 | | m*g* rms |
| | $T_A$ = 25°C, no filtering, Z axis | | 7.5 | | m*g* rms |
| Noise Density | $T_A$ = 25°C, no filtering, X axis and Y axis | | 0.2 | | m*g*/√Hz rms |
| | $T_A$ = 25°C, no filtering, Z axis | | 0.3 | | m*g*/√Hz rms |
| 3 dB Bandwidth | | | 330 | | Hz |
| Sensor Resonant Frequency | | | 5.5 | | kHz |
| Self-Test Change in Output Response | X axis and Y axis | 500 | 1100 | 1700 | LSB |
| | Z axis | 90 | 450 | 860 | LSB |
| INCLINOMETER | | | | | |
| Sensitivity | | | 0.044 | | °/LSB |
| TEMPERATURE SENSOR | | | | | |
| Scale Factor | $T_A$ = 25°C output = 0x0000 | | 0.14 | | °C/LSB |

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ADC INPUT | | | | | |
| Resolution | | | 12 | | Bits |
| Integral Nonlinearity | | | ±2 | | LSB |
| Differential Nonlinearity | | | ±1 | | LSB |
| Offset Error | | | ±4 | | LSB |
| Gain Error | | | ±2 | | LSB |
| Input Range | | 0 | | +3.3 | V |
| Input Capacitance | During acquisition | | 20 | | pF |
| DAC OUTPUT | 5 kΩ/100 pF to GND | | | | |
| Resolution | | | 12 | | Bits |
| Relative Accuracy | For Code 101 to Code 4095 | | ±4 | | LSB |
| Differential Nonlinearity | | | ±1 | | LSB |
| Offset Error | | | ±5 | | mV |
| Gain Error | | | ±0.5 | | % |
| Output Range | | 0 | | +3.3 | V |
| Output Impedance | | | 2 | | Ω |
| Output Settling Time | | | 10 | | µs |
| LOGIC INPUTS[1] | | | | | |
| Input High Voltage, $V_{INH}$ | | 2.0 | | | V |
| Input Low Voltage, $V_{INL}$ | | | | 0.8 | V |
| | $\overline{CS}$ signal to wake up from sleep mode | | | 0.55 | V |
| $\overline{CS}$ Wake-Up Pulse Width | | 20 | | | µs |
| Logic 1 Input Current, $I_{INH}$ | $V_{IH}$ = 3.3 V | | ±0.2 | ±10 | µA |
| Logic 0 Input Current, $I_{INL}$ | $V_{IL}$ = 0 V | | | | |
| All Pins Except $\overline{RST}$ | | | −40 | −60 | µA |
| $\overline{RST}$ Pin | | | −1 | | mA |
| Input Capacitance, $C_{IN}$ | | | 10 | | pF |
| DIGITAL OUTPUTS[1] | | | | | |
| Output High Voltage, $V_{OH}$ | $I_{SOURCE}$ = 1.6 mA | 2.4 | | | V |
| Output Low Voltage, $V_{OL}$ | $I_{SINK}$ = 1.6 mA | | | 0.4 | V |
| FLASH MEMORY | Endurance[2] | 10,000 | | | Cycles |
| Data Retention[3] | $T_J$ = 85°C | 20 | | | Years |
| FUNCTIONAL TIMES[4] | Time until data is available | | | | |
| Power-On Start-up Time | Normal mode, SMPL_PRD ≤ 0x09 | | 180 | | ms |
| | Low power mode, SMPL_PRD ≥ 0x0A | | 245 | | ms |
| Reset Recovery Time | Normal mode, SMPL_PRD ≤ 0x09 | | 55 | | ms |
| | Low power mode, SMPL_PRD ≥ 0x0A | | 120 | | ms |
| Sleep Mode Recovery Time | | | 2.5 | | ms |
| Flash Memory Test Time | Normal mode, SMPL_PRD ≤ 0x09 | | 17 | | ms |
| | Low power mode, SMPL_PRD ≥ 0x0A | | 90 | | ms |
| Automatic Self-Test Time | | | 12 | | ms |
| CONVERSION RATE | SMPL_PRD = 0x01 to 0xFF | 0.413 | | 819.2 | SPS |
| Clock Accuracy | | | | ±3 | % |
| Sync Input Clock | | | | 1.2 | kHz |
| POWER SUPPLY | Operating voltage range, VCC | 4.75 | 5.0 | 5.25 | V |
| Power Supply Current | Low power mode at 25°C | | 18 | | mA |
| | Normal mode at 25°C | | 42 | | mA |
| | Sleep mode at 25°C | | 500 | | µA |

[1] The digital I/O signals are driven by an internal 3.3 V supply, and the inputs are 5 V tolerant.
[2] Endurance is qualified as per JEDEC Standard 22, Method A117, and measured at −40°C, +25°C, +85°C, and +125°C.
[3] The retention lifetime equivalent is at a junction temperature ($T_J$) of 85°C as per JEDEC Standard 22, Method A117. Retention lifetime decreases with junction temperature.
[4] These times do not include thermal settling and internal filter response times (330 Hz bandwidth), which may impact overall accuracy.

## TIMING SPECIFICATIONS

$T_A$ = 25°C, VCC = 5 V, unless otherwise noted.

**Table 2.**

| Parameter | Description | Normal Mode (SMPL_PRD ≤ 0x09) | | | Low Power Mode (SMPL_PRD ≥ 0x0A) | | | Burst Mode | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min[1] | Typ | Max | Min[1] | Typ | Max | Min[1] | Typ | Max | |
| $f_{SCLK}$ | | 0.01 | | 2.0 | 0.01 | | 0.3 | 0.01 | | 1.0 | MHz |
| $t_{STALL}$ | Stall period between data | 9 | | | 75 | | | $1/f_{SCLK}$ | | | µs |
| $t_{READRATE}$ | Read rate | 40 | | | 100 | | | | | | us |
| $t_{CS}$ | Chip select to clock edge | 48.8 | | | 48.8 | | | 48.8 | | | ns |
| $t_{DAV}$ | DOUT valid after SCLK edge | | | 100 | | | 100 | | | 100 | ns |
| $t_{DSU}$ | DIN setup time before SCLK rising edge | 24.4 | | | 24.4 | | | 24.4 | | | ns |
| $t_{DHD}$ | DIN hold time after SCLK rising edge | 48.8 | | | 48.8 | | | 48.8 | | | ns |
| $t_{SCLKR}$, $t_{SCLKF}$ | SCLK rise/fall times | | 5 | 12.5 | | 5 | 12.5 | | 5 | 12.5 | ns |
| $t_{DF}$, $t_{DR}$ | DOUT rise/fall times | | 5 | 12.5 | | 5 | 12.5 | | 5 | 12.5 | ns |
| $t_{SFS}$ | $\overline{CS}$ high after SCLK edge | 5 | | | 5 | | | 5 | | | ns |
| $t_1$ | Input sync pulse width | | 5 | | | | | | | | µs |
| $t_2$ | Input sync to data ready output | | 600 | | | | | | | | µs |
| $t_3$ | Input sync period | 833 | | | | | | | | | µs |

[1]Guaranteed by design and characterization, but not tested in production.

## TIMING DIAGRAMS

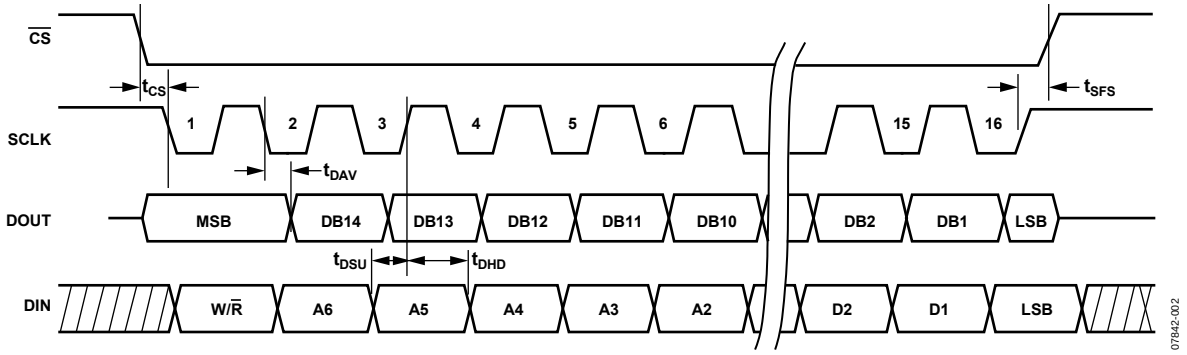



*Figure 2. SPI Timing and Sequence*

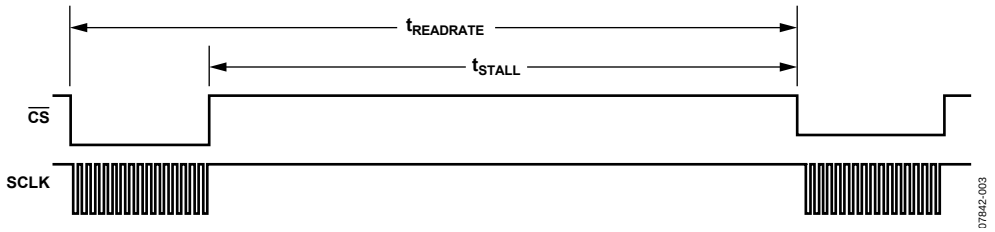



*Figure 3. Stall Time and Data Rate*

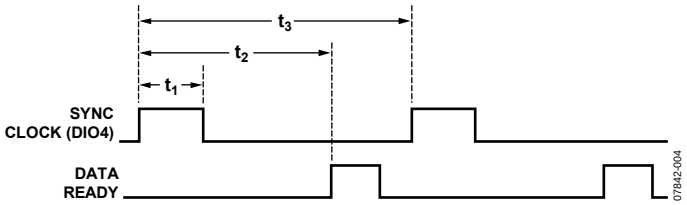



*Figure 4. Input Clock Timing Diagram*

# ABSOLUTE MAXIMUM RATINGS

**Table 3.**

| Parameter | Rating |
|---|---|
| Acceleration | |
| Any Axis, Unpowered | 2000 *g* |
| Any Axis, Powered | 2000 *g* |
| VCC to GND | −0.3 V to +6.0 V |
| Digital Input Voltage to GND | −0.3 V to +5.3 V |
| Digital Output Voltage to GND | −0.3 V to VCC + 0.3 V |
| Analog Input to GND | −0.3 V to +3.6 V |
| Operating Temperature Range | −40°C to +85°C |
| Storage Temperature Range | −65°C to +125°C[1, 2] |

[1] Extended exposure to temperatures outside the specified temperature range of −40°C to +85°C can adversely affect the accuracy of the factory calibration. For best accuracy, store the parts within the specified operating range of −40°C to +85°C.

[2] Although the device is capable of withstanding short-term exposure to 150°C, long-term exposure threatens internal mechanical integrity.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 4. Package Characteristics**

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Device Weight |
|---|---|---|---|
| 24-Lead Module | 39.8°C/W | 14.2°C/W | 16 grams |

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

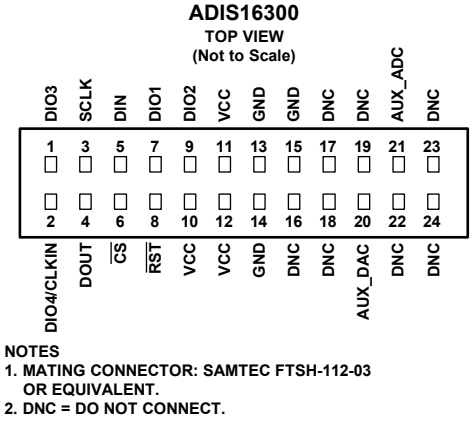
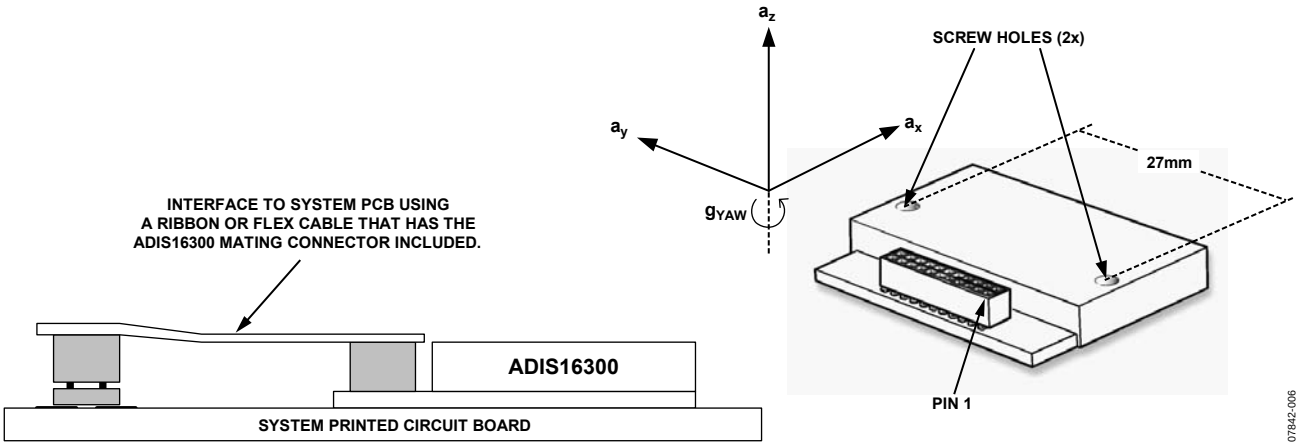



*Figure 5. Pin Configuration*




NOTES
1. ACCELERATION ($a_X$, $a_Y$, $a_Z$) AND ROTATIONAL ($g_{YAW}$) ARROWS INDICATE THE DIRECTION OF MOTION THAT PRODUCES A POSITIVE OUTPUT.

*Figure 6. Device Orientation, Mounting, and Interface Diagrams*

**Table 5. Pin Function Descriptions**

| Pin No. | Mnemonic | Type[1] | Description |
|---|---|---|---|
| 1 | DIO3 | I/O | Configurable Digital Input/Output. |
| 2 | DIO4/CLKIN | I/O | Configurable Digital Input/Output or Sync Clock Input. |
| 16, 17, 18, 19, 22, 23, 24 | DNC | N/A | Do Not Connect. |
| 3 | SCLK | I | SPI Serial Clock. |
| 4 | DOUT | O | SPI Data Output. Clocks output on SCLK falling edge. |
| 5 | DIN | I | SPI Data Input. Clocks input on SCLK rising edge. |
| 6 | $\overline{CS}$ | I | SPI Chip Select. |
| 7 | DIO1 | I/O | Configurable Digital Input/Output. |
| 8 | $\overline{RST}$ | I | Reset. |
| 9 | DIO2 | I/O | Configurable Digital Input/Output. |
| 10, 11, 12 | VCC | S | Power Supply. |
| 13, 14, 15 | GND | S | Power Ground. |
| 20 | AUX_DAC | O | Auxiliary, 12-Bit DAC Output. |
| 21 | AUX_ADC | I | Auxiliary, 12-Bit ADC Input. |

[1] S is supply, O is output, I is input, N/A is not applicable.

# TYPICAL PERFORMANCE CHARACTERISTICS

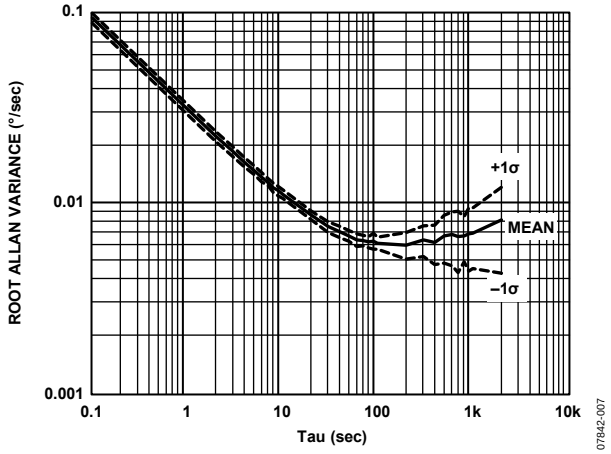



*Figure 7. Gyroscope Allan Variance*

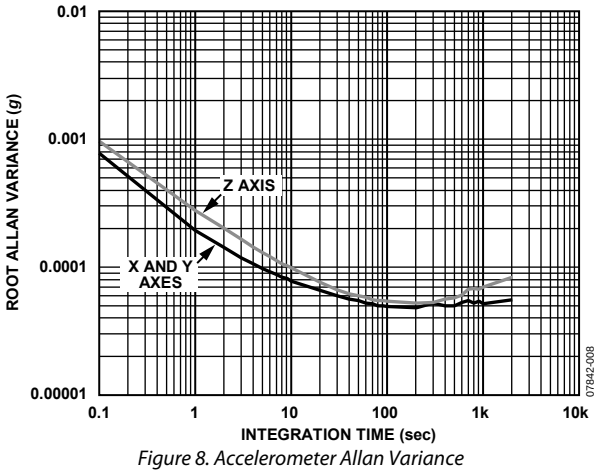



*Figure 8. Accelerometer Allan Variance*

# BASIC OPERATION

The ADIS16300 is an autonomous sensor system that starts up after it has a valid power supply voltage and begins producing inertial measurement data at a sample rate of 819.2 SPS. After each sample cycle, the sensor data loads into the output registers and DIO1 pulses, providing a new-data-ready control signal for driving system-level interrupt service routines. In a typical system, a master processor accesses the output data registers through the SPI interface, using the hook-up shown in Figure 9. Table 6 provides a generic, functional description for each pin on the master processor. Table 7 describes the typical master processor settings normally found in a configuration register and used for communicating with the ADIS16300.

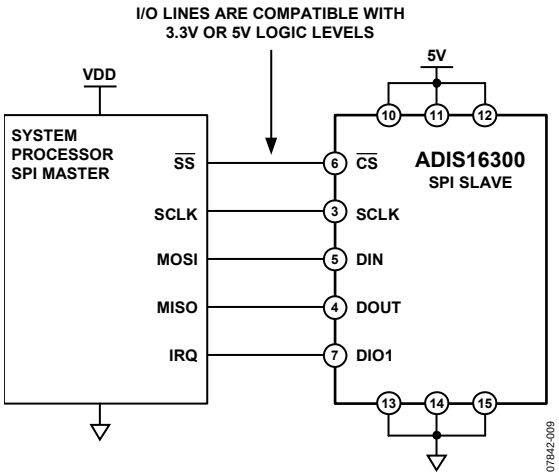



*Figure 9. Electrical Hook-Up Diagram*

**Table 6. Generic Master Processor Pin Names and Functions**

| Pin Name | Function |
|---|---|
| $\overline{SS}$ | Slave select |
| IRQ | Interrupt request |
| MOSI | Master output, slave input |
| MISO | Master input, slave output |
| SCLK | Serial clock |

**Table 7. Generic Master Processor SPI Settings**

| Processor Setting | Description |
|---|---|
| Master | The ADIS16300 operates as a slave. |
| SCLK Rate ≤ 2 MHz[1] | Normal mode, SMPL_PRD[7:0] ≤ 0x08. |
| CPOL = 1 | Clock polarity. |
| CPHA = 1 | Clock phase. |
| MSB-First | Bit sequence. |
| 16-Bit | Shift register/data length. |

[1] For burst mode, SCLK rate ≤ 1 MHz. For low power mode, SCLK rate ≤ 300 kHz.

The user registers provide addressing for all input/output operations on the SPI interface. Each 16-bit register has two 7-bit addresses: one for its upper byte and one for its lower byte. Table 8 provides the lower-byte address for each register, and Figure 10 provides the generic bit assignments.

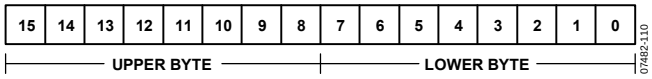



*Figure 10. Output Register Bit Assignments*

## READING SENSOR DATA

Although the ADIS16300 produces data independently, it operates as an SPI slave device, which communicates with system (master) processors using the 16-bit segments displayed in Figure 11. Individual register reads require two 16-bit sequences. The first 16-bit sequence provides the read command bit (R/W = 0) and the target register address (A6…A0). The second sequence transmits the register contents (D15…D0) on the DOUT line. For example, if DIN= 0x0A00, then the content of XACCL_OUT shifts out on the DOUT line during the next 16-bit sequence.

The SPI operates in full duplex mode, which means that the master processor can read the output data from DOUT while using the same SCLK pulses to transmit the next target address on DIN.

## DEVICE CONFIGURATION

The user register memory map (see Table 8) identifies configuration registers with either a W or R/W. Configuration commands also use the bit sequence displayed in Figure 12. If the MSB is equal to 1, the last eight bits (DC7...DC0) in the DIN sequence load into the memory address associated with the address bits (A5...A0). For example, if the DIN = 0xA11F, then 0x1F loads into Address Location 0x26 (ALM_MAG1, upper byte) at the conclusion of the data frame.

Most of the registers have a backup location in nonvolatile flash memory. The master processor must manage the backup function. Set GLOB_CMD[3] = 1 (DIN = 0xBE01) to execute a manual flash update (backup) operation, which copies the user registers into their respective flash memory locations. This operation takes 50 ms and requires the power supply voltage to be within the specified limit to complete properly. The FLASH_CNT register provides a running count of these events for managing the long-term reliability of the flash memory.

## BURST MODE DATA COLLECTION

Burst mode data collection offers a more process-efficient method for collecting data from the ADIS16300. In 10 sequential data cycles (each separated by one SCLK period), all nine output registers clock out on DOUT. This sequence starts when the DIN sequence is 0011 1110 0000 0000 (0x3E00). Next, the contents of each output register are output from DOUT, starting with SUPPLY_OUT and ending with AUX_ADC (see Figure 12). The addressing sequence shown in Table 8 determines the order of the outputs in burst mode.

**Table 8. User Register Memory Map**

| Name | R/W | Flash Backup | Address[1] | Default | Function | Bit Assignments |
|---|---|---|---|---|---|---|
| FLASH_CNT | R | Yes | 0x00 | N/A | Flash memory write count | N/A |
| SUPPLY_OUT | R | No | 0x02 | N/A | Power supply measurement | Table 9 |
| GYRO_OUT | R | No | 0x04 | N/A | X-axis gyroscope output | Table 9 |
| N/A | N/A | N/A | 0x06 | N/A | Reserved | N/A |
| N/A | N/A | N/A | 0x08 | N/A | Reserved | N/A |
| XACCL_OUT | R | No | 0x0A | N/A | X-axis accelerometer output | Table 9 |
| YACCL_OUT | R | No | 0x0C | N/A | Y-axis accelerometer output | Table 9 |
| ZACCL_OUT | R | No | 0x0E | N/A | Z-axis accelerometer output | Table 9 |
| TEMP_OUT | R | No | 0x10 | N/A | X-axis gyroscope temperature measurement | Table 9 |
| PITCH_OUT | R | No | 0x12 | N/A | X-axis inclinometer output measurement | Table 9 |
| ROLL_OUT | R | No | 0x14 | N/A | Y-axis inclinometer output measurement | Table 9 |
| AUX_ADC | R | No | 0x16 | N/A | Auxiliary ADC output | Table 9 |
| N/A | N/A | N/A | 0x18 | N/A | Reserved | N/A |
| GYRO_OFF | R/W | Yes | 0x1A | 0x0000 | X-axis gyroscope bias offset factor | Table 10 |
| N/A | N/A | N/A | 0x1C | N/A | Reserved | N/A |
| N/A | N/A | N/A | 0x1E | N/A | Reserved | N/A |
| XACCL_OFF | R/W | Yes | 0x20 | 0x0000 | X-axis acceleration bias offset factor | Table 11 |
| YACCL_OFF | R/W | Yes | 0x22 | 0x0000 | Y-axis acceleration bias offset factor | Table 11 |
| ZACCL_OFF | R/W | Yes | 0x24 | 0x0000 | Z-axis acceleration bias offset factor | Table 11 |
| ALM_MAG1 | R/W | Yes | 0x26 | 0x0000 | Alarm 1 amplitude threshold | Table 22 |
| ALM_MAG2 | R/W | Yes | 0x28 | 0x0000 | Alarm 2 amplitude threshold | Table 22 |
| ALM_SMPL1 | R/W | Yes | 0x2A | 0x0000 | Alarm 1 sample size | Table 23 |
| ALM_SMPL2 | R/W | Yes | 0x2C | 0x0000 | Alarm 2 sample size | Table 23 |
| ALM_CTRL | R/W | Yes | 0x2E | 0x0000 | Alarm control | Table 24 |
| AUX_DAC | R/W | No | 0x30 | 0x0000 | Auxiliary DAC data | Table 18 |
| GPIO_CTRL | R/W | No | 0x32 | 0x0000 | Auxiliary digital input/output control | Table 16 |
| MSC_CTRL | R/W | Yes | 0x34 | 0x0006 | Miscellaneous control | Table 17 |
| SMPL_PRD | R/W | Yes | 0x36 | 0x0001 | Internal sample period (rate) control | Table 13 |
| SENS_AVG | R/W | Yes | 0x38 | 0x0402 | Dynamic range/digital filter control | Table 15 |
| SLP_CNT | W | No | 0x3A | 0x0000 | Sleep mode control | Table 14 |
| DIAG_STAT | R | No | 0x3C | 0x0000 | System status | Table 21 |
| GLOB_CMD | W | N/A | 0x3E | 0x0000 | System command | Table 12 |

[1] Each register contains two bytes. The address of the lower byte is displayed. The address of the upper byte is equal to the address of the lower byte, plus 1.

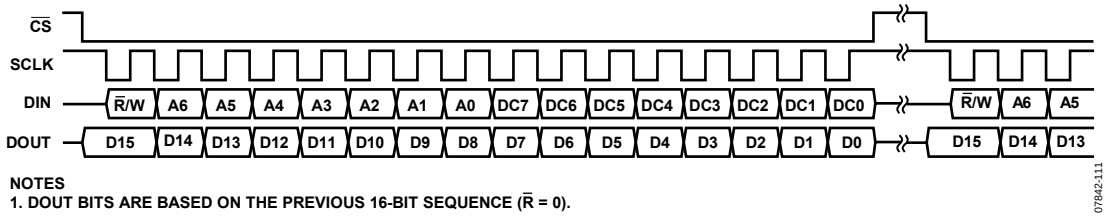



*Figure 11. Output Register Bit Assignments*

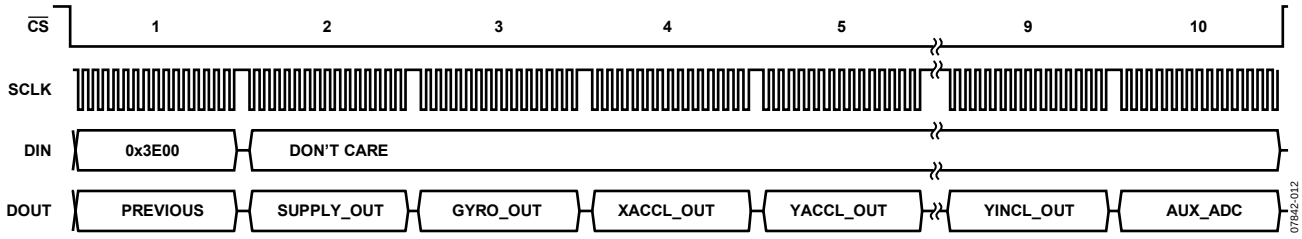



*Figure 12. Burst Mode Read Sequence*

## OUTPUT DATA REGISTERS

Figure 6 provides the positive measurement direction for each inertial sensor (gyroscope and accelerometers). Table 9 provides the configuration and scale factor for each output data register in the ADIS16300. All inertial sensor outputs are 14-bits in length and are in twos complement format, which means that 0x0000 is equal to 0 LSB, 0x0001 is equal to +1 LSB, and 0x3FFF is equal to −1 LSB. The following is an example of how to calculate the sensor measurement from the GYRO_OUT:

$$\text{GYRO\_OUT} = 0\text{x}3\text{B}4\text{A}$$

$$0\text{x}000 - 0\text{x}33\text{B}4\text{A} = -0\text{x}04\text{B}6 = -(4 \times 256 + 11 \times 16 + 6)$$

$$-0\text{x}04\text{B}6 = -1206 \text{ LSB}$$

$$\text{Rate} = 0.05°/\text{sec} \times (-1206) = -60.3°/\text{sec}$$

Therefore, a GYRO_OUT output of 0x3B4A corresponds to a clockwise rotation about the z-axis (see Figure 6) of 60.3°/sec when looking at the top of the package.

**Table 9. Output Data Register Formats**

| Register | Bits | Format | Scale |
|---|---|---|---|
| SUPPLY_OUT | 12 | Binary, 5 V = 0x0814 | 2.42 mV |
| GYRO_OUT[1] | 14 | Twos complement | 0.05°/sec |
| XACCL_OUT | 14 | Twos complement | 0.6 m*g* |
| YACCL_OUT | 14 | Twos complement | 0.6 m*g* |
| ZACCL_OUT | 14 | Twos complement | 0.6 m*g* |
| TEMP_OUT | 12 | Twos complement<br>25°C = 0x0000 | 0.14°C |
| ROLL_OUT | 13 | Twos complement | 0.044° |
| PITCH_OUT | 13 | Twos complement | 0.044° |
| AUX_ADC | 12 | Binary, 1 V = 0x04D9 | 0.81 mV |

[1] Assumes that the scaling is set to ± 300°/sec. This factor scales with the range.

Each output data register uses the bit assignments shown in Figure 13. The ND flag indicates that unread data resides in the output data registers. This flag clears and returns to 0 during an output register read sequence. It returns to 1 after the next internal sample updates the registers with new data. The EA flag indicates that one of the error flags in the DIAG_STAT register (see Table 21) is active (true). The remaining 14-bits are for data.

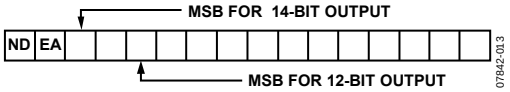



*Figure 13. Output Register Bit Assignments*

### *Inclinometers*

The ROLL_OUT and PITCH_OUT registers provide a tilt angle calculation, based on the accelerometers. The zero reference is the point at which the z-axis faces gravity for a north-east-down (NED) configuration.

$$ROLL\_OUT = a\tan\left(\frac{YACCL\_OUT}{ZACCL\_OUT}\right) = \phi$$

$$PITCH\_OUT = a\tan\left(\frac{-XACCL\_OUT}{YACCL\_OUT\ x\ \sin(\phi) + ZACCL\_OUT\ x\ \cos(\phi)}\right)$$

### *Auxiliary ADC*

The AUX_ADC register provides access to the auxiliary ADC input channel. The ADC is a 12-bit successive approximation converter, which has an equivalent input circuit to the one in Figure 14. The maximum input range is +3.3 V. The ESD protection diodes can handle 10 mA without causing irreversible damage. The switch on-resistance (R1) has a typical value of 100 Ω. The sampling capacitor, C2, has a typical value of 16 pF.

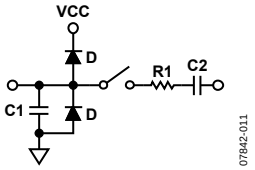



*Figure 14. Equivalent Analog Input Circuit (Conversion Phase: Switch Open, Track Phase: Switch Closed)*

## CALIBRATION

### *Manual Bias Calibration*

The bias offset registers in Table 10 and Table 11 provide a manual adjustment function for the output of each sensor. For example, if GYRO_OFF equals 0x1FF6, the GYRO_OUT offset shifts by −10 LSBs, or −0.125°/sec. The DIN command for the upper byte is DIN = 0x9B1F; for the lower byte, DIN = 0x9AF6.

**Table 10. GYRO_OFF**

| Bits | Description |
|---|---|
| [15:13] | Not used. |
| [12:0] | Data bits. Twos complement, 0.0125°/sec per LSB.<br>Typical adjustment range = ±50°/sec. |

**Table 11. XACCL_OFF, YACCL_OFF, ZACCL_OFF**

| Bits | Description |
|---|---|
| [15:12] | Not used. |
| [11:0] | Data bits, twos complement 0.6 m*g*/LSB.<br>Typical adjustment range = ±1.2 *g*. |

### *Gyroscope Automatic Bias Null Calibration*

Set GLOB_CMD[0] = 1 (DIN = 0xBE01) to execute this function, which measures GYRO_OUT and then loads GYRO_OFF with the opposite value to provide a quick bias calibration. Then, all sensor data resets to zero, and the flash memory updates automatically (50 ms). See Table 12.

### *Gyroscope Precision Automatic Bias Null Calibration*

Set GLOB_CMD[4] = 1 (DIN = 0xBE10) to execute this function, which takes the sensor offline for 30 seconds while it collects a set of GYRO_OUT data and calculates a more accurate bias correction factor. Once calculated, the correction factor loads into GYRO_OFF, all sensor data resets to zero, and the flash memory updates automatically (50 ms). See Table 12.

### *Restoring Factory Calibration*

Set GLOB_CMD[1] = 1 (DIN = 0xBE02) to execute this function, which resets each user calibration register (see Table 10 and Table 11) to 0x0000, resets all sensor data to zero, and automatically updates the flash memory (50 ms). See Table 12.

### *Linear Acceleration Bias Compensation (Gyroscope)*

Set MSC_CTRL[7] = 1 (DIN = 0xB486) to enable correction for low frequency acceleration influences on gyroscope bias. Note that the DIN sequence also preserves the factory default condition for the data ready function (see Table 17).

## OPERATIONAL CONTROL

### *Global Commands*

The GLOB_CMD register provides trigger bits for several useful functions. Setting the assigned bit to 1 starts each operation, which returns to the bit to 0 after completion. For example, set GLOB_CMD[7] = 1 (DIN = 0xBE80) to execute a software reset, which stops the sensor operation and runs the device through its start-up sequence. This includes loading the control registers with their respective flash memory locations prior to producing new data. Reading the GLOB_CMD registers (DIN = 0x3E00) starts the burst mode read sequence.

**Table 12. GLOB_CMD**

| Bits | Description |
|---|---|
| [15:8] | Not used |
| [7] | Software reset command |
| [6:5] | Not used |
| [4] | Precision autonull command |
| [3] | Flash update command |
| [2] | Auxiliary DAC data latch |
| [1] | Factory calibration restore command |
| [0] | Autonull command |

### *Internal Sample Rate*

The ADIS16300 performs best when the sample rate is set to the factory default setting of 819.2 SPS. For applications that value lower sample rates, the SMPL_PRD register controls the ADIS16300 internal sample (see Table 13), and the following relationship produces the sample rate:

$$t_S = t_B \times N_S + 1$$

**Table 13. SMPL_PRD**

| Bit | Description |
|---|---|
| [15:8] | Not used |
| [7] | Time base ($t_B$)<br>0 = 0.61035 ms, 1 = 18.921 ms |
| [6:0] | Increment setting ($N_S$)<br>Internal sample period = $t_S = t_B \times N_S + 1$ |

For example, set SMPL_PRD[7:0] = 0x0A (DIN = 0xB60A) for an internal sample period of 6.7 ms (sample rate = 149 SPS). For systems that value lower sample rates, in-system characterization can help determine performance trade-offs.

### *Power Management*

Setting SMPL_PRD ≥ 0x0A also sets the sensor in low power mode. In addition to sensor performance, this mode also affects SPI data rates (see Table 2). Two sleep mode options are listed in Table 14. Set SLP_CNT[8] = 1 (DIN = 0xBB01) to start the indefinite sleep mode, which requires $\overline{CS}$ assertion (high to low), reset, or power cycle to wake-up. Set SLP_CNT[7:0] = 0x64 (DIN = 0xBA64) to put the ADIS16300 to sleep for 100 seconds, as an example of the programmable sleep time option.

**Table 14. SLP_CNT**

| Bit | Description |
|---|---|
| [15:9] | Not used |
| [8] | Indefinite sleep mode, set to 1 |
| [7:0] | Programmable time bits, 0.5 sec/LSB |

### *Digital Filtering*

The signal conditioning circuit of each sensor has a typical analog bandwidth of 350 Hz. A programmable Bartlett window FIR filter provides an opportunity for additional noise reduction on all output data registers. SENS_AVG[2:0] controls the number of taps according to the equation in Table 15. For example, set SENS_AVG[2:0] = 110 (DIN = 0xB806) to establish a 129-tap setting.

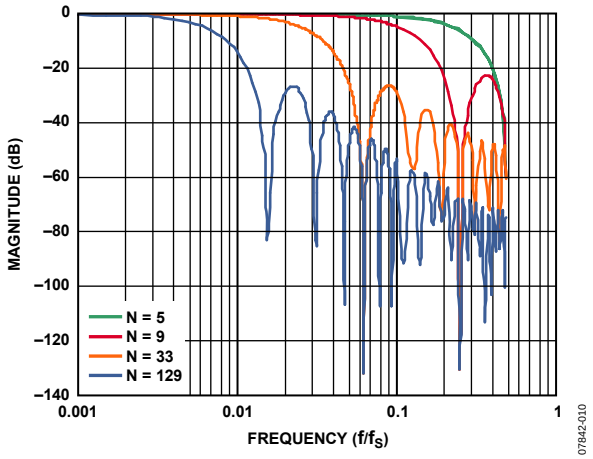



*Figure 15. Bartlett Window FIR Frequency Response*

### *Dynamic Range*

There are three dynamic range settings for the gyroscope: ±75°/sec, ±150°/sec, and ±300°/sec. The lower dynamic range settings (±75°/sec and ±150°/sec) limit the minimum filter tap sizes to maintain the resolution as the measurement range decreases. The recommended order for programming the SENS_AVG register is upper byte (sensitivity), followed by lower byte (filtering). For example, set SENS_AVG[10:8] = 010 (DIN = 0xB902) for a measurement range to ±150°/sec.

**Table 15. SENS_AVG**

| Bits | Value | Description |
|---|---|---|
| [15:11] | | Not used |
| [10:8] | | Measurement range (sensitivity) selection |
| | 100 | ±300°/sec (default condition) |
| | 010 | ±150°/sec, filter taps ≥ 4 (Bits[2:0] ≥ 0x02) |
| | 001 | ±75°/sec, filter taps ≥ 16 (Bits[2:0] ≥ 0x04) |
| [7:3] | | Not used |
| [2:0] | | Filter tap setting, number of taps<br>$N = 2^M+1$ for M > 0, N = 1 for M = 0 |

## INPUT/OUTPUT FUNCTIONS

### *General-Purpose I/O*

DIO1, DIO2, DIO3, and DIO4 are configurable, general-purpose I/O lines that serve multiple purposes according to the following control register priority: MSC_CTRL, ALM_CTRL, and GPIO_CTRL. For example, set GPIO_CTRL = 0x080C (DIN = 0xB508, then 0xB40C) to set DIO1 and DIO2 as inputs and DIO3 and DIO4 as outputs, with DIO3 set low and DIO4 set high.

**Table 16. GPIO_CTRL**

| Bit | Description |
|---|---|
| [15:12] | Not used |
| [11] | General-Purpose I/O Line 4 (DIO4) data level |
| [10] | General-Purpose I/O Line 3 (DIO3) data level |
| [9] | General-Purpose I/O Line 2 (DIO2) data level |
| [8] | General-Purpose I/O Line 1 (DIO1) data level |
| [7:4] | Not used |
| [3] | General-Purpose I/O Line 4 (DIO4), direction control<br>1 = output, 0 = input |
| [2] | General-Purpose I/O Line 3 (DIO3), direction control<br>1 = output, 0 = input |
| [1] | General-Purpose I/O Line 2 (DIO2), direction control<br>1 = output, 0 = input |
| [0] | General-Purpose I/O Line 1 (DIO1), direction control<br>1 = output, 0 = input |

### *Input Clock Configuration*

The input clock configuration function allows for external control over sampling in the ADIS16300. Set GPIO_CTRL[3] = 0 (DIN = 0x0B200) and SMPL_PRD[7:0] = 0x00 (DIN = 0xB600) to enable this function. See Table 2 and Figure 4 for timing information.

### *Data Ready I/O Indicator*

The factory default sets DIO1 as a positive data ready indicator signal. The MSC_CTRL[2:0] register provides configuration options for changing this. For example, set MSC_CTRL[2:0] = 100 (DIN = 0xB404) to change the polarity of the data ready signal for interrupt inputs that require negative logic inputs for activation. The pulse width will be between 100 µs and 200 µs over all conditions.

**Table 17. MSC_CTRL**

| Bits | Description |
|---|---|
| [15:12] | Not used |
| [11] | Memory test (clears on completion)<br>1 = enabled, 0 = disabled |
| [10] | Internal self-test enable (clears on completion)<br>1 = enabled, 0 = disabled |
| [9] | Manual self-test, negative stimulus<br>1 = enabled, 0 = disabled |
| [8] | Manual self-test, positive stimulus<br>1 = enabled, 0 = disabled |
| [7] | Linear acceleration bias compensation for gyroscopes<br>1 = enabled, 0 = disabled |
| [6] | Linear accelerometer origin alignment<br>1 = enabled, 0 = disabled |
| [5:3] | Not used |
| [2] | Data ready enable<br>1 = enabled, 0 = disabled |
| [1] | Data ready polarity<br>1 = active high, 0 = active low |
| [0] | Data ready line select<br>1 = DIO2, 0 = DIO1 |

### *Auxiliary DAC*

The 12-bit AUX_DAC line can drive its output to within 5 mV of the ground reference when it is not sinking current. As the output approaches 0 V, the linearity begins to degrade (~100 LSB beginning point). As the sink current increases, the nonlinear range increases. The DAC latch command moves the values of the AUX_DAC register into the DAC input register, enabling both bytes to take effect at the same time.

**Table 18. AUX_DAC**

| Bit | Description |
|---|---|
| [15:12] | Not used |
| [11:0] | Data bits, scale factor = 0.8059 mV/code<br>Offset binary format, 0 V = 0 codes |

**Table 19. Setting AUX_DAC = 1V**

| DIN | Descripition |
|---|---|
| 0XB0D9 | AUX_DAC[7:0] = 0xD9 (217 LSB). |
| 0xB104 | AUX_DAC[15:8] = 0x04 (1024 LSB). |
| 0xBE04 | GLOB_CMD[2] = 1.<br>Move values into the DAC input register, resulting in a 1 V output level. |

## DIAGNOSTICS

### *Self-Test*

Self-test offers the opportunity to verify the mechanical integrity of each MEMS sensor. It applies an electrostatic force to each sensor element, which results in mechanical displacement that simulates a response to actual motion. Table 1 lists the expected response for each sensor, which provides pass/fail criteria. Set MSC_CTRL[10] = 1 (DIN = 0xB504) to run the internal self-test routine, which exercises all inertial sensors, measures each response, makes pass/fail decisions, and reports them to error flags in the DIAG_STAT register. MSC_CTRL[10] resets itself to 0 after completing the routine. MSC_CTRL[9:8] (DIN = 0xB502 or 0xB501) provides manual control over the self-test function. Table 20 gives an example test flow for using this option.

**Table 20. Manual Self-Test Example Sequence**

| DIN | Description |
|---|---|
| 0xB601 | SMPL_PRD[7:0] = 0x01, sample rate = 819.2 SPS. |
| 0xB904 | SENS_AVG[15:8] = 0x04, gyro range = ±300°/sec. |
| 0xB802 | SENS_AVG[7:0] = 0x02, 4-tap averaging filter. |
| | Delay = 50 ms. |
| 0x0400 | Read GYRO_OUT. |
| 0x0600 | Read XACCL_OUT. |
| 0x0800 | Read YACCL_OUT. |
| 0x0A00 | Read ZACCL_OUT. |
| 0xB502 | MSC_CTRL[9] = 1, gyroscope negative self-test. |
| | Delay = 50 ms. |
| 0x0400 | Read GYRO_OUT. |
| | Determine whether the bias in the gyroscope output changes according to the expectation set in Table 2. |
| 0xB501 | MSC_CTRL[9:8] = 01, gyroscope/accelerometer positive self-test. |
| | Delay = 50 ms. |
| 0x0400 | Read GYRO_OUT. |
| 0x0600 | Read XACCL_OUT. |
| 0x0800 | Read YACCL_OUT. |
| 0x0A00 | Read ZACCL_OUT |
| | Determine whether the bias in the gyroscope and accelerometers changed according to the expectation set in Table 2. |
| 0xB500 | MSC_CTRL[15:8] = 0x00. |

Zero motion provides results that are more reliable. The settings in Table 20 are flexible and provide opportunity for optimization around speed and noise influence. For example, lowering the filtering taps enables lower delay times but increases the opportunity for noise influence.

### *Memory Test*

Setting MSC_CTRL[11] = 1 (DIN = 0xB508) does a check-sum verification of the flash memory locations. The pass/fail criteria load into the DIAG_STAT[6] register.

### *Status*

The error flags provide indicator functions for common system level issues. All of the flags clear (set to 0) after each DIAG_STAT register read cycle. If an error condition remains, the error flag returns to 1 during the next sample cycle. DIAG_STAT[1:0] does not require a read of this register to return to zero. If the power supply voltage goes back into range, these two flags clear automatically.

**Table 21. DIAG_STAT Bit Descriptions**

| Bit | Description |
|---|---|
| [15] | Z-axis accelerometer self-test failure<br>1 = error condition, 0 = normal operation |
| [14] | Y-axis accelerometer self-test failure<br>1 = error condition, 0 = normal operation |
| [13] | X-axis accelerometer self-test failure<br>1 = error condition, 0 = normal operation |
| [12:11] | Not used |
| [10] | Gyroscope self-test failure<br>1 = error condition, 0 = normal operation |
| [9] | Alarm 2 status<br>1 = active, 0 = inactive |
| [8] | Alarm 1 status<br>1 = active, 0 = inactive |
| [7] | Not used |
| [6] | Flash test, check-sum flag<br>1 = failure, 0 = normal operation |
| [5] | Self-test diagnostic error flag<br>1 = error condition, 0 = normal operation |
| [4] | Sensor overrange<br>1 = error condition, 0 = normal operation |
| [3] | SPI communications failure<br>1 = error condition, 0 = normal operation |
| [2] | Flash update failed<br>1 = error condition, 0 = normal operation |
| [1] | Power supply above 5.25 V<br>1 = power supply ≥ 5.25 V, 0 = power supply ≤ 5.25 V |
| [0] | Power supply below 4.75 V<br>1 = power supply ≤ 4.75 V, 0 = power supply ≥ 4.75 V |

### *Alarm Registers*

The alarm function provides monitoring for two independent conditions. The ALM_CTRL register provides control inputs for data source, data filtering (prior to comparison), static comparison, dynamic rate-of-change comparison, and output indicator configurations. The ALM_MAGx registers establish the trigger threshold and polarity configurations.

Table 25 gives an example of how to configure a static alarm.

The ALM_SMPLx registers provide the numbers of samples to use in the dynamic rate-of-change configuration. The period equals the number in the ALM_SMPLx register, multiplied by the sample period time, established by the SMPL_PRD register. See Table 26 for an example of how to configure the sensor for this type of function.

**Table 22. ALM_MAG1, ALM_MAG2**

| Bit | Description |
|---|---|
| [15] | Comparison polarity<br>1 = greater than, 0 = less than |
| [14] | Not used |
| [13:0] | Data bits that match the format of the trigger source selection |

**Table 23. ALM_SMPL1, ALM_SMPL2**

| Bit | Description |
|---|---|
| [15:8] | Not used |
| [7:0] | Data bits: number of samples (both 0x00 and 0x01 = 1) |

**Table 24. ALM_CTRL Bit Designations**

| Bits | Value | Description |
|---|---|---|
| [15:12] | | Alarm 2 source selection |
| | 0000 | Disable |
| | 0001 | Power supply output |
| | 0010 | Gyroscope output |
| | 0011 | Not used |
| | 0100 | Not used |
| | 0101 | X-axis accelerometer output |
| | 0110 | Y-axis accelerometer output |
| | 0111 | Z-axis accelerometer output |
| | 1000 | Gyroscopes temperature output |
| | 1001 | X-axis inclinometer output |
| | 1010 | Y- axis inclinometer output |
| | 1011 | Auxiliary ADC input |
| [11:8] | | Alarm 1 source selection (same as Alarm 2) |
| [7] | | Rate of change (ROC) enable for Alarm 2<br>1 = rate of change, 0 = static level |
| [6] | | Rate of change (ROC) enable for Alarm 1<br>1 = rate of change, 0 = static level |
| [5] | | Not used |
| [4] | | Comparison data filter setting[1]<br>1 = filtered data, 0 = unfiltered data |
| [3] | | Not used |
| [2] | | Alarm output enable<br>1 = enabled, 0 = disabled |
| [1] | | Alarm output polarity<br>1 = active high, 0 = active low |
| [0] | | Alarm output line select<br>1 = DIO2, 0 = DIO1 |

[1] Incline outputs always use filtered data in this comparison.

**Table 25. Alarm Configuration Example 1**

| DIN | Description |
|---|---|
| 0xAF55 | ALM_CTRL = 0x5517. |
| 0xAE17 | Alarm 1 input = XACCL_OUT.<br>Alarm 2 input = XACCL_OUT.<br>Static level comparison, filtered data.<br>DIO2 output indicator, positive polarity. |
| 0xA783 | ALM_MAG1 = 0x8341. |
| 0xA641 | Alarm 1 is true if XACCL_OUT > 0.5 *g*. |
| 0xA93C | ALM_MAG2= 0x3CBF. |
| 0xA8BF | Alarm 2 is true if XACCL_OUT < –0.5 *g*. |

**Table 26. Alarm Configuration Example 2**

| DIN | Description |
|---|---|
| 0xAF76 | ALM_CTRL = 0x7687. |
| 0xAE87 | Alarm 1 input = ZACCL_OUT.<br>Alarm 2 input = YACCL_OUT.<br>Rate of change comparison, unfiltered data.<br>DIO2 output indicator, positive polarity. |
| 0xB601 | SMPL_PRD = 0x0001.<br>Sample rate = 819.2 SPS. |
| 0xAB08 | ALM_SMPL1 = 0x0008.<br>Alarm 1 rate of change period = 9.77 ms. |
| 0xAC50 | ALM_SMPL2= 0x0050.<br>Alarm 2 rate of change period = 97.7 ms. |
| 0xA783 | ALM_MAG1 = 0x8341. |
| 0xA641 | Alarm 1 is true if XACCL_OUT > 0.5 *g*. |
| 0xA93C | ALM_MAG2= 0x3CBE. |
| 0xA8BE | Alarm 2 is true if XACCL_OUT < –0.5 *g*. |

# OUTLINE DIMENSIONS

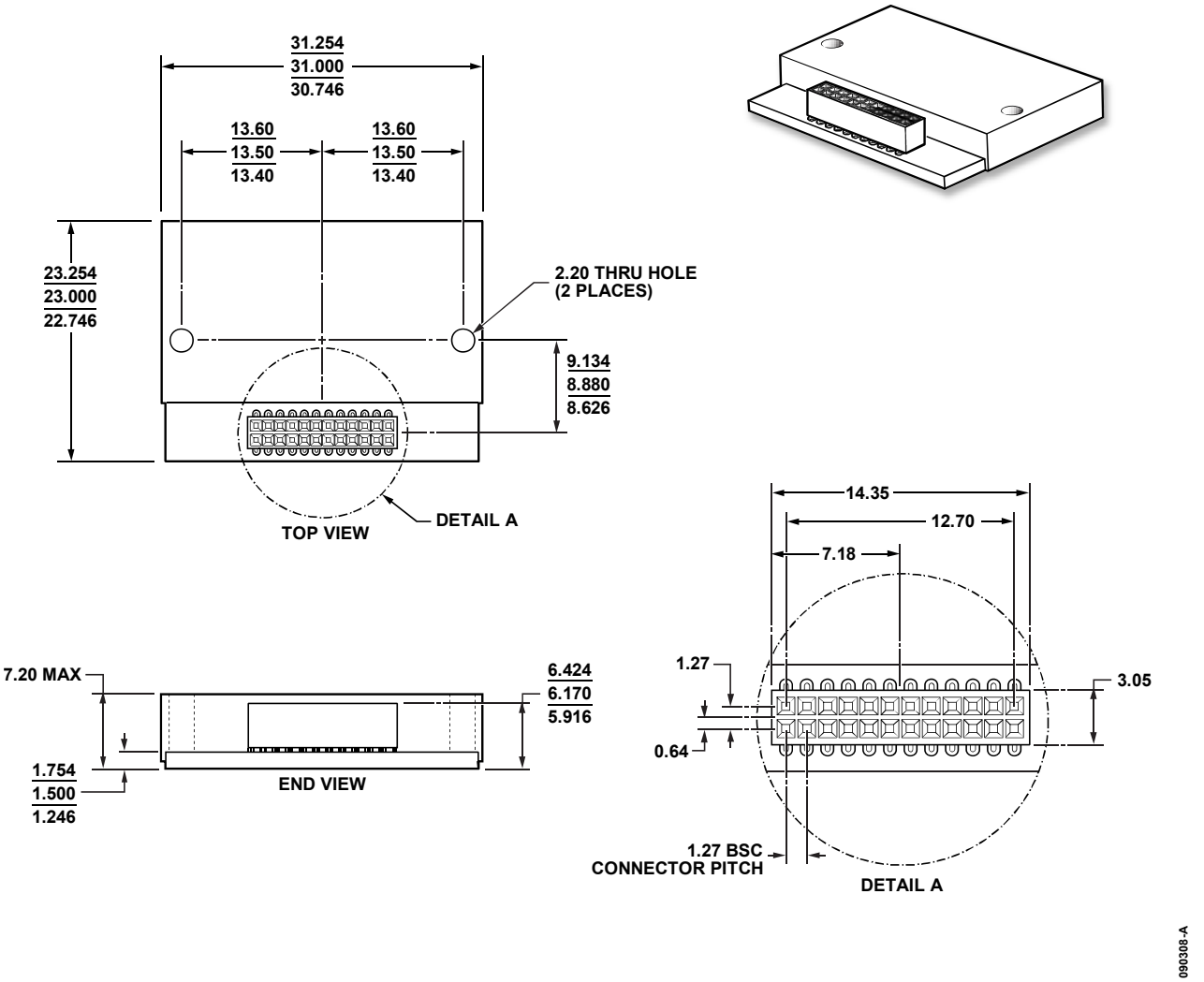



*Figure 16. 24-Lead Module with Connector Interface*
*(ML-24-4)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| ADIS16300AMLZ[1] | −40°C to +85°C | 24-Lead Module with Connector Interface | ML-24-4 |

[1] Z = RoHS Compliant Part.


D07842-0-4/09(A)